

# Development of a High-Speed Digital Signal-Process Board for the KEKB Bunch Feedback Systems

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## Abstract

We have been developing bunch feedback systems to cure expected coupled bunch instabilities in KEKB, a b-Factory project in Japan. In KEKB, the number of stored bunches amounts to  $\sim 5000$  per ring and their spacing is only 2 nano-seconds. In order to treat these bunches each part of the feedback systems should be very wide-banded. The signal process part of these feedback systems is a digital system to ensure the reliability under the severe condition. We developed a prototype of a digital signal process board consisting of an analog-to-digital converter, a main signal process part and a digital-to-analog converter. In the main signal process part, custom-made de-multiplexer/multiplexer IC's are implemented to reduce the frequency in the logic. The logic works as both simple digital delay and a two-tap FIR filter with a flexible tap configuration.

## 1 INTRODUCTION

At KEK Japan, a large accelerator facility, KEKB, is now under construction. The features of KEKB are

- Consists of two large rings (3020 meters in circumference) with an injector
- Very short bunch spacing, 2 nano-seconds
- A large number of accelerating cavities .

We estimated growth rates of the various modes of coupled bunch instabilities based on the design studies of accelerating cavities and other accelerator components. The result is that the growth rates of the some modes are not negligibly small. To cure these instabilities, we are now developing bunch-by-bunch feedback systems both in the longitudinal and transverse planes. In this article, we will describe the signal process part of these bunch feedback systems.

## 2 DESIGN OF THE SIGNAL PROCESS PART

### 2.1 General Remarks

In designing the feedback systems, we adopted the bunch-by-bunch scheme rather than the mode-by-mode scheme. Conceptually speaking, this means that there is one feedback system for each individual bunch. Consequently, much resource, sometimes a large number of identical parts, should be used to realize these feedback systems.

In general, if one construct many identical systems, it is recommended that the system may constructed with digital

technique. Following this guiding principle, we adopted the digital signal process system. Recent progresses of fast A-to-D converter (ADC) technology support this decision.

### 2.2 What the signal process part must do?

The signal process part may have to do two things: one is signa-delay which corresponds to phase rotation through 90 degrees, the other is noise elimination (when necessary). If the bunch-by-bunch position-signal is contaminated with non-negligible noises, we must filter out them with some mechanism. In our case, the noise reduction would be done by the digital filter technique. A straightforward way to estimate the noise is to measure them actually. For this end, we made beam experiments in TRISTAN Main Ring by using the front-end electronics which we have already developed. The results of these experiments were reported elsewhere[1] and our finding was that the noise level is lower than the signal by about  $-40$  dB<sup>1</sup>. From this fact, we found that the signal process part needs not to have a significant noise-elimination capability.

### 2.3 Reduction of the signal-rate by a custom gate array

From the above discussion, we decided to make a simple digital delay. However, even though it is simple, the design is not easy because the bunch frequency is very high, 500 MHz, and the number of bunches are very large, about 5000. The requirements of a very high signal-rate and large amount of memory are conflicting at the present stage of ordinary IC technology.

Then we have chosen a strategy of making order-made gate arrays for the signal-rate reduction. Several companies have a technology of GaAs gate arrays for very high frequency signal process. One of them, Oki Electric Industry co., Ltd., fabricated a GaAs special IC which is capable of de-multiplexing signal of hundreds MHz to that of 1/16 of the original frequency (order of 10 MHz). Naturally, the counter part of this IC, that can multiplex the signal of a lower frequency to that of the original frequency can be constructed with the same technology. Fabrication of such custom IC is, of course, rather costly. But thanks to these IC's, the design of other parts of the circuitry becomes much less difficult. The typical frequency outside of the IC is order of 10 MHz, namely, the ordinary CMOS level.

<sup>1</sup>The term noise, here, does not include DC offset.

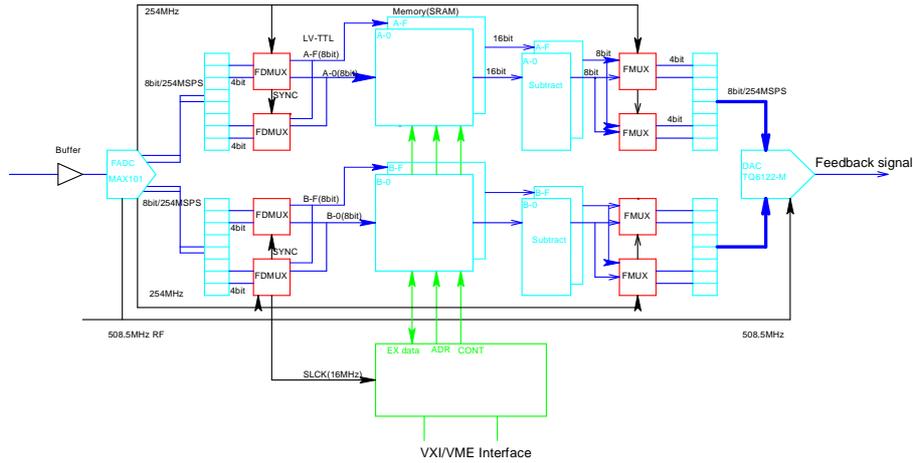


Figure 1: Block diagram of the signal process board.

Owing to this relatively lower signal rate, we can make very simple digital filter, the 2-tap filters. F. Pedersen[2] first discussed these 2-tap filters for the feedback business. After that we carefully investigated the feasibility of applying them to the bunch feedback systems.[3] One can not expect the 2-tap filter to have a sophisticated filter power, but he/she can expect it to be able to eliminate the constant (DC) level. This DC-elimination power is sometimes very attractive for us. Recent our experiments[4] of the feedback based on the 2 tap filter shows the power of this method clearly.

To realize this 2-tap filter, we must prepare 2 arrays of the memory instead of one array which would be necessary for a simple digital delay. In addition, we must prepare a simple logic, which accomplishes subtract operation. This is done by a field programmable gate arrays (FPGA).

#### 2.4 Data flow in the signal process board

Figure 1 shows data-flow on the signal process board. An analog signal is converted to a digital one by 500 MHz ADC whose output is interleaved, namely, we get two 250 MHz digital signal from 2 output ports, alternatively. Corresponding to each port, there are 4 de-multiplexers which degrade the signal-rate from 250 MHz to  $\sim 16$  MHz. These data are stored in 2 series of memory array, named *A* and *B*. The FPGA subtracts the content of array *A* from the content of array *B*, that is the operation of the 2-tap filter. The results of the subtractions are multiplexed with the 4 multiplexers. At last the DAC converts the data into an analog signal. Mode selection, 2-tap mode or direct (simple) delay mode and the tap position control is done by another FPGA.

### 3 ORGANIZATION OF THE CIRCUIT BOARDS

Our basic plan is to make a signal process system with only one board in order to minimize the data exchange between boards. However, it is impossible to make it with only one board if we want to put a large number of the memory IC's

on a reasonable (that is, not extremely big) size of board. Thus we decided to make the system with a relatively large mother board with some daughter boards attached to it.

#### 3.1 The mother board

The mother board has the size of 366.71 mm (height)  $\times$  460 mm (depth). The height is the 3 units of the euro card but the depth is non-standard. On this board, the ADC daughter-board, 16 memory daughter-boards, an FPGA for general control and 4 de-multiplexer/multiplexer chip pairs are mounted. Figure 2 shows the mother board and the daughter boards on it.

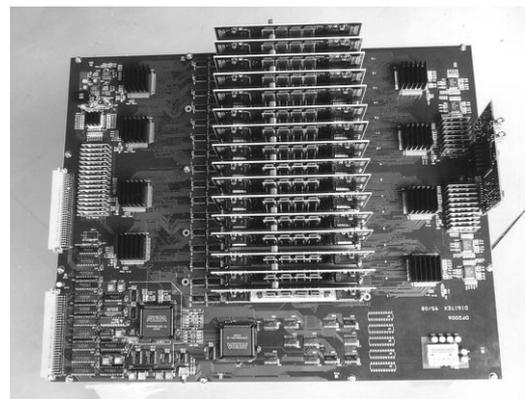


Figure 2: The mother board. In this picture, the signal flows from the right to the left.

The photograph in Fig 3 shows the close view of the de-multiplexer and multiplexer chips. The left one is the de-multiplexer and the right one is the multiplexer. Each chip (de-)multiplexes 4-bit data, then 2 chips together (de-)multiplex 8 bit data.

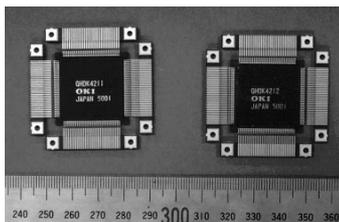


Figure 3: The custom gate array ICs. The left one is the demultiplexer while the right one is the multiplexer.

### 3.2 The ADC daughter-board

Several companies have released ADC chips of 500 MHz conversion rate with 8-bit resolution. We adopted MAX101 for our purpose at present stage. Recent progresses in the flush-ADC technology is remarkable and we can expect that some new versions of such ADC's will be released. Then, in order to make our system flexible to fit the new versions, the ADC is put on a separate daughter-board.

### 3.3 The memory-board

When we use the system as a 2-tap filter we must prepare 2 series of the memory for each bunch. One series of the memory must have the size of the number of turns corresponding to 3/4 cycle of the bunch oscillation. In the longitudinal plane, one cycle is about 100 turns, then we must prepare at least 75 bytes for one bunch. It is reasonable to prepare 100 bytes for one bunch considering margin. Then the necessary memory size is  $5120 \times 100 \times 2 = 1\text{Mbytes}$ .

Practically, the capacity of commercial memory-chips are not so small. We use the chips of 32kbytes and these chips are mounted on the 16 daughter-boards.

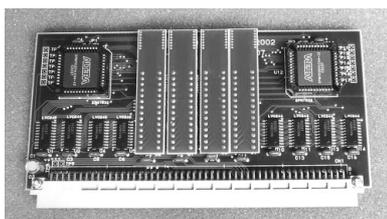


Figure 4: The daughter board for the memory IC's. Also the FPGA for the subtract operation is mounted on this board.

### 3.4 Interface and control

As we mentioned previously, the board has a non-standard size. In order to communicate this system, a VME interface will be prepared. Through this interface, we set the modes (2-tap or simple delay), the tap-position information, which are necessary when it is used as the 2-tap filter, and some general control signals.

### 3.5 A byproduct

If we replace the 2-tap filter part of the board with a large amount of memory, it can be a transient memory which records the behavior of each bunch over thousand of turns. This can be a powerful tool of the accelerator physics.

Our practical plan is that we install a bank of memory of 20 Mbytes which is able to store of the data of 4096 turns of 5120 bunches. The number of turns 4096 is about 2 times longitudinal radiation damping time in Low Energy Ring.

## 4 HOW TO USE THIS BOARD

As we explained previously, the board works as a high speed digital delay capable of dealing with 5120 bunches. In addition, it can work as 2-tap digital filter also dealing with 5120 bunches. We plan to use this board both for the longitudinal and transverse planes. As we discussed in the previous paper[3] the 2-tap filter scheme works very well in the longitudinal plane. Then the board will work as the 2-tap filter in this plane. The DC-elimination characteristic of the 2-tap filter can suppress the non-necessary power consumption in the longitudinal kicker.

In the transverse plane, on the contrary, we will use the board as the simple digital delay. If there is no elements which can cause the phase jump of the betatron oscillation, the 2-tap filter feedback works very well[3]. This is experimentally confirmed by the feedback system in CESR at Cornell[5], and our recent experiments[6]. But if there are some sources which introduce a sudden jump of phase of the betatron oscillation, it is not recommended to use the 2-tap filter scheme[7]. The heavy beam-beam collision and some impedance sources are the candidates of these sources. In KEKB, the tune shift due to the beam-beam collision goes to 0.05. In that case, the phase jump will not be negligibly small and there is some possibility that the 2-tap filter scheme can fail.

## 5 REFERENCES

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